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Coaxially Gated In-Wire Thin-Film Transistors Made by Template Assembly

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A key issue in the realization of nano- and molecular-scale electronics is the development of strategies for making devices that can be assembled into circuits.[1−5] In the case of transistor-based circuits, useful architectures allow each component device to be individually gated.[2−5] Logic circuits and nonvolatile memory have now been assembled from carbon nanotubes[3] and semiconductor nanowires.[4−6] In the latter case, field-effect transistors (FETs) are made from cross-point nanowire junctions[4] or core−multishell nanowire structures.[5] The crossing nanowire or metal contact evaporated on the outer shell acts as the local gate contact. An important potential advantage of multishell-nanowire-based FETs is that they already embody the "wrap-around gate" projected for future scaling of conventional silicon transistors.[7,8]

This paper demonstrates a "wrap-around gate" approach to nanoscale thin-film transistors (TFTs). We describe the synthesis and characterization of coaxially gated in-wire TFTs. These devices consist of a cadmium chalcogenide thin film sandwiched between metal wire segments within a SiO_2 tube. The synthesis involves the surface sol−gel (SSG) deposition of SiO_2 tubes on the pore walls of an alumina (anodic aluminum oxide, AAO) membrane[9] and electroplating of the composite nanowires within the tubes.[10] This approach is simple and scalable, with precise control over the diameter, segment lengths, and dielectric thickness. Another advantage of the coaxially gated TFT structure is full encapsulation of the semiconductor segment, which prevents its oxidation.

In-wire TFTs were prepared as shown in Figure 1. First, the Ag-backed AAO membrane is subjected to deposition of SiO_2 nanotubes on the pore walls by repeating $SiCl_4$ adsorption−hydrolysis cycles.[9] The membrane is then used as the cathode in an electrochemical cell to electroplate 3−5-μm-long Au segments inside the SiO_2 tubes. Semiconductor thin-film segments are grown on the tip of the Au wire using electrochemically induced CdS film growth[11,12] or cyclic voltametric CdSe deposition.[10] The top Au segments, 3−5 μm long, are electroplated onto the cadmium chalcogenide films. Finally, the Au/CdS(Se)/Au@$(SiO_2)_n$ (where n is the number of SSG cycles used for SiO_2 tube growth) nanowires are released by dissolving the Ag backing and AAO membrane. Metal/CdS/metal nanowires with different semiconductor segment lengths are prepared using 1-h and 15-min deposition times. In the latter case, Ag clusters were chemically deposited prior to electrodeposition of the top metal segment in order to ensure good electrical contact. These devices are referred to as Au/CdS/Au@$(SiO_2)_{10}$ and Au/CdS/AgAu@$(SiO_2)_{14}$, respectively.

An optical micrograph and TEM images of the in-wire TFT structures are shown in Figure 2a−c. The Au/CdS/Au junctions are clearly seen, and their thickness can be roughly estimated at 100−200 nm for the wires prepared by using 1-h CdS deposition.

For the 15-min CdS deposition, TEM images show an approximate CdS film thickness at 30−50 nm. An AFM image of a 31-nm-thick CdS film prepared the same way on a planar Au substrate shows densely packed 20−50-nm grains. An XRD pattern of the planar CdS film (not shown) shows one CdS-related peak at $2\Theta = 26.65°$ ($d = 3.34$ Å), the position of which corresponds to the (111) reflection of the cubic zinc blende structure ($d = 3.36$ Å) or the (002) reflection of the hexagonal wurzite structure ($d = 3.36$ Å). However, the absence of other strong peaks from the (100) and (101) planes of the hexagonal phase indicates that CdS crystallizes mainly in the cubic phase, in contrast to the hexagonal phase formed on ITO and SnO_2 substrates.[11] The average crystal size estimated from the X-ray line widths is 39.6 nm, which is consistent with the AFM data.

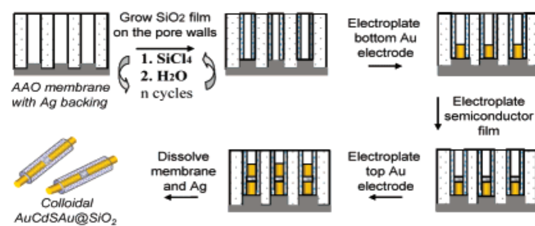

Figure 1. Template synthesis of coaxially gated in-wire TFTs.

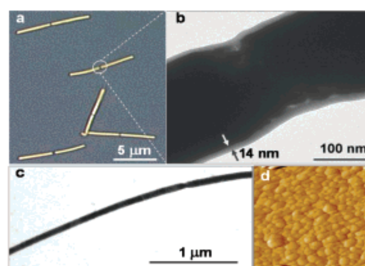

Figure 2. Optical micrograph (a) and TEM images (b,c) of Au/CdS/Au@$(SiO_2)_{10}$ nanowires prepared in AAO membranes with pore size 280 ± 20 nm (a,b) and 70 ± 10 nm (c). (d) Tapping-mode AFM image (585 × 585 nm, Z range 30.0°) of a CdS film grown on an Au-coated glass substrate using the electrochemically induced deposition technique.

The thickness of the SiO_2 tubes that encapsulate the nanowires is uniform along the wire length and ranges from 12 to 14 nm for 10 SSG cycles (Figure 2b) and from 16 to 18 nm for 14 SSG cycles. The flexibility of these shells allows them to precisely follow the shape of Au/CdS/Au junctions (Figure 2b), thus enabling good adhesion of the gate dielectric to the semiconductor film.

The nanowires were aligned as shown in Figure 3a for electrical measurements (see Supporting Information). $I_{DS}-V_{DS}$ characteristics of Au/CdS/Au@$(SiO_2)_{10}$ and Au/CdS/AgAu@$(SiO_2)_{14}$ devices are shown in Figure 3b,c. At zero gate bias ($V_{GS} = 0$), turn-on potentials are −0.6 and −0.2 V, respectively, which is in reasonable agreement with the differences between the electron affinity of CdS (∼4.5 eV) and the Au (∼5.2 eV) and Ag (∼4.7 eV) work functions, respectively. The Au/CdS/AgAu@$(SiO_2)_{14}$ devices show a zero gate bias DS resistivity 55 times lower than that of Au/CdS/Au@$(SiO_2)_{10}$, which may be attributed to better CdS/Ag electrical contact due to the formation of Ag−S bonds, and possibly to fewer grain

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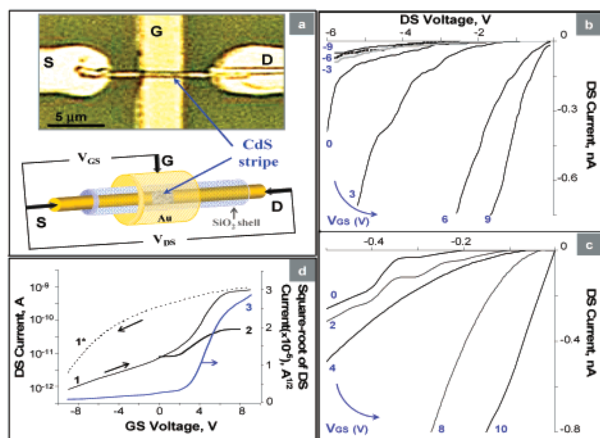

Figure 3. (a) Optical micrograph and schematic drawing of the test structure and Au/CdS/Au@$(SiO_2)_{10}$ nanowire aligned for measurement of electrical properties. Letters S, D, and G indicate source, drain, and gate electrodes, respectively. (b,c) Typical $I_{DS}-V_{DS}$ characteristics of in-wire TFTs for different values of gate voltage (V_{GS}): (b) Au/CdS/Au@$(SiO_2)_{10}$//Au (CdS deposition for 1 h), 11 devices measured; (c) Au/CdS/AgAu@-$(SiO_2)_{14}$//Au (CdS deposition for 15 min), 9 devices measured. Variation in zero gate DS current values was ±10%. Gate leakage currents were $10^{-14}-10^{-12}$ A. (d) $I_{DS}-V_{GS}$ characteristics of in-wire TFTs: log I_{DS} (1, 1*) and $\sqrt{I_{DS}}$ (3) for Au/CdS/Au@$(SiO_2)_{10}$//Au at $V_{DS} = -2$V for a gate sweep from −9 to 9 V (1) and vice versa (1*); (2) log I_{DS} for Au/CdSe/Au@$(SiO_2)_{14}$//Au at $V_{DS} = 5$ V for a gate sweep from 0 to 8 V, 4 devices measured.

boundaries in the thinner CdS film. However, the metal/semiconductor contacts of the in-wire TFTs are still much more resistive than those of planar TFTs.[13,14] This implies a stronger effect of the contact resistance on the nanowire device properties. Therefore, all characteristics described below result from a field effect on both the CdS channel and Au(Ag)/CdS contacts.

The $I_{DS}-V_{DS}$ characteristics of both devices clearly show a field effect, which is more pronounced at negative drain voltage (Figure 3b,c). At $V_{DS} = -2$ V, the Au/CdS/Au@$(SiO_2)_{10}$ devices have an ON/OFF current ratio of 10^3, a threshold voltage of 2.4 V, and a subthreshold slope of 2.2 V/decade (Figure 3d, traces 1 and 3). The Au/CdS/AgAu@$(SiO_2)_{14}$ devices show similar parameters at $V_{DS} = -0.2$ V and a gate sweep from 0 to 10 V. While the in-wire TFTs can operate at relatively low drain voltages, the above parameters are superior to those found with planar CdS[13] and nanocrystal-derived CdSe[14a] TFTs in the gate voltage range ±9−10 V. The lower V_T and a 3-fold decrease in the subthreshold slope (S) relative to planar nanocrystal-derived CdSe TFTs ($S = 7-10$ V/decade[14a]) may result from the thinner dielectric layer and coaxial gating. A similar tendency was predicted for planar double-gated vs conventional FETs.[7] On the other hand, the channel mobility of the in-wire TFTs is approximately $(5 \pm 2) \times 10^{-5}$ cm^2 V^{-1} s^{-1}. This is 4−6 orders of magnitude lower than that found for TFTs with several-micrometer-long channels of planar nanocrystal-derived and vapor-deposited CdSe and CdS.[13,14] To a certain extent, this decrease may be caused by the significant reduction of the channel length in the in-wire TFTs. The field-dependent mobility decrease is a predicted consequence of FET channel scaling.[7,15] However, high Schottky contact resistance is most likely responsible for the low apparent mobility values. We believe that much higher mobility values can be achieved by further improving the metal/semiconductor interfaces and grain structure of the semiconductor segment, as well as by using metal contacts with lower work functions. Au/CdSe/Au@$(SiO_2)_{14}$ TFTs show poorer performance, with an ON/OFF current ratio about 10 (Figure 3d, trace 2). This is consistent with observation by other groups[14] that planar CdSe TFTs fabricated without annealing exhibit very weak, if any, field effect.

Log(I_{DS})−V_{GS} graphs with a gate sweep from −9 to 9 V and vice versa (Figure 3d, traces 1 and 1*) show CCW hysteresis contrary to the CW one observed with planar CdSe TFTs.[14] The origin of the hysteresis is not currently understood but may be tentatively ascribed to trap states at the semiconductor/SiO_2 interface.[14] However, the chemical nature of the traps in our wet-assembled in-wire devices may differ from that in the thermally evaporated or annealed planar TFTs. Also, a field effect on the Au/CdS contact properties may cause the CCW hysteresis. Oxidation of the planar TFTs[14a] is a less likely source of trap states in this case because the in-wire TFTs are encapsulated by SiO_2.

In summary, coaxially gated in-wire CdS and CdSe thin-film transistors can be made by using a combination of templated surface sol−gel and electrochemical deposition techniques. The CdS-based TFTs can operate at drain voltages lower than 1 V and show better ON/OFF current ratio, threshold voltage, and subthreshold slope than chemically similar planar TFTs. While the devices described here were not optimized for performance, one might expect significant improvements by using strategies that have been developed or predicted for conventional FETs and TFTs.[7,13,15] The control of dimensions afforded by the template synthesis should make it possible to reduce the gate dielectric thickness, channel length, and diameter of the semiconductor body (see, e.g., Figure 2c). The latter would extend the gate effect across the body region[7] and might also result in the formation of single-crystal semiconductor segments.[12] The SSG technique should allow substitution of higher K dielectrics, such as zirconium, titanium, and tantalum oxides for SiO_2.[16] Finally, thermal annealing of the semiconductor segment prior to top electrode deposition is expected to improve the performance of the CdSe-based devices.

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Supporting Information Available: Experimental details of TFT synthesis, transistor structure assembly, and electrical measurements. This material is available free of charge via the Internet at http://pubs.acs.org.

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